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(b) By using the gate array platform given in Fig. 1.30, implement the CMOS circuit as compactly as possible with the aspect ratio, which is the ratio of vertical dimension to horizontal dimension, as close to 1 as possible. Solution Manual for CMOS Digital Integrated Circuits Analysis and Design 4th Edition by Kang

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1.1 An ADD/SUBTRACT logic circuit is shown in Fig. P1.1. It performs the ADD operation for P = 0 and SUBTRACT for P = 1. Figure P1.1 (a) Draw an equivalent CMOS logic diagram by noting that most ...

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